#7A/3-17-04 L. Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OFFICIAL

In re application of GEORG FARKAS	Atty. Docket CH 000018
Serial: 09/932,086	Group Art Unit: 2133
Filed: 08/17/2001	Examiner: ENG, MARSHALL S J

ARRANGEMENT FOR TESTING INTEGRATED CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. 1.111

Sir:

Responsive to the Office Action of January 28, 2004, please amend this application as follows:

IN THE CLAIMS

1. (Cancel) An arrangement for testing integrated circuits, including

a1 a test system (2) which includes a test vector generator (4) for generating test vectors, and